Customer No.: 31561
Application No.: 10/605,253
Docket No.: 11649-US-PA

REMARKS

Present Status of the Application

The Office Action (OA) mailed on September 27, 2004 asserts that claims 1-19 of Group I are drawn to semiconductor process and claims 20-30 of Group II to device. Hence, Applicants are required to elect one group under 35 U.S.C. 121. Moreover, if Group I is elected, electing a single species among Species 1 (claims 1-10) and Species 2 (claims 11-19) is required for lacking a generic claim for Group I. Similarly, if Group II is elected instead, it is also required to elect a single species among Species 1 (claims 20-24) and Species 2 (claims 25-30).

In response thereto, Applicants have *withdrawn Group 2, elected Group 1* **and** *further elected Species 1 of Group I with traverse.* **However, Applicants have amended claims 1 and 6 to make claim 1 be a generic claim in Group 1, and respectfully request withdrawal of the further restriction requirement to claims 1-19 of Group I.**

Applicants' Election

In response to the Restriction Requirement, Applicants have elected Group I and further elected Species 1 of Group I, which corresponds to claims 1-10 and FIGs. 1A-1C and 2A-2C.

The non-elected Species 2 of Group I corresponds to claims 11-19 and FIGs. 3A-3D and 4A-4F. In addition, the non-elected Group II corresponds to claims 20-30 and the figures.

Discussion of Restriction Requirements to Group I

Applicants submit that with the above amendments, *Species 1 and 2 of Group 1 no more need to be divided* under 35 U.S.C. 121, since claim 1 has been amended to be a generic claim. Amended claim 1 is generic to independent claims 11 and 15 of Species 2 for the reasons below.

Firstly, the subject matter of amended claim 1 is a method for forming an *OTP-ROM cell* that is illustrated in FIGs. 1A-1C, and the subject matter of claim 11 or 15 is a method for forming an *OTP-ROM array* that is illustrated in FIGs. 3A-3D or 4A-4F. As indicated by paragraph [0008] and the figures, it is obvious that the process of forming a mono-level or multi-level OTP-ROM array is *entirely based* on the process of forming a single OTP-ROM cell, since each memory cell in the mono-level or multi-level OTP-ROM array is formed in a manner substantially the same as the single OTP-ROM cell is formed. Therefore, all elements of claim 1 are included in claims 11 and 15, i.e., claims 11 and 15 are derived from claim 1, so that claim 1 of Species 1 is generic to independent claims 11 and 15 of Species 2.

Moreover, in claim language, the meaning of the article "a/an" is not limited to "one", but also means "more than one" or even "a plurality of" *when each one is substantially the same.* **Therefore, the scope of claim 1 includes the following claim 1', in which the differences from claim 1 are indicated by [ ] (deletion) and underlines (addition):**

1'. A method form forming [a] a plurality of OTP-ROM cells, comprising:

forming [a] a plurality of stacked structures on a substrate, wherein [the] each stacked structure comprises, from bottom to top, a first doped layer, a dielectric layer and a nucleation layer;

forming an insulating layer over the substrate, the insulating layer having [an] a plurality of openings therein exposing [a portion] portions of the nucleation layer;

forming [a] a plurality of second doped layers of polysilicon or amorphous silicon in the openings; and

performing an annealing process to convert portions of the second doped layers into [a] a plurality of first single-crystal silicon layers,

wherein one of the first doped layers and the second doped layers is P-doped, and the other is N-doped.

Presence of the words "portions of" in claim 1' does not make claim 1' exceed the scope of claim 1, which will be explained later.

Applicants submit that claim 1 is generic to claim 11, because claim 1' derived from claim 1 is generic to claim 11. To prove this, the steps of claims 1' and 11 are compared as follows:

1. The step of

"forming a plurality of stacked structures on a substrate, wherein each stacked structure comprises, from bottom to top, a first doped layer, a dielectric layer and a nucleation layer"

of claim 1' is generic to step (a) of claim 11:

"(a) providing a substrate having an insulating layer and linear stacked structures formed thereon, wherein the linear stacked structures are embedded in trenches of the insulating layer, and each linear stacked layer includes, from bottom to top, a semiconductor layer of a first conductivity type, an anti-fuse layer and a nucleation layer".

Specifically, the stacked structures of claim 1' are generic to the linear stacked structures of claim 11, the first doped layer of claim 1' is generic to the semiconductor layer of a first conductivity type of claim 11, and the dielectric layer of claim 1' is generic to the anti-fuse layer of claim 11.

2. The step of

"forming an insulating layer over the substrate, the insulating layer having a plurality of openings therein exposing portions of the nucleation layer"

of claim 1' is generic to steps (b) and (c) of claim 11:

"(b) forming a next insulating layer over the substrate; (c) forming a plurality of trenches in the next insulating layer in an orientation different from an orientation of the trenches in the former insulating layer, so that multi-portions of each nucleation layer are exposed"

wherein *a trench can be considered as one type of opening*, **as recognized in the art.**

3. The step of

"forming a plurality of second doped layers of polysilicon or amorphous silicon in the openings"

of claim 1' is generic to step (d) of claim 11:

"(d) filling a polysilicon layer of a second conductivity type into each trench in the next insulating layer"

4. The step of

"performing an annealing process to convert portions of the second doped layers into a plurality of first single-crystal silicon layers"

of claim 1' is substantially the same as step (e) of claim 11:

"(e) performing an annealing process to convert portions of the polysilicon layers on the nucleation layers into single-crystal silicon layers"

It is noted that restricting "portions of" the second doped layers to be converted into single-crystal silicon layers in claim 1' does not make claim 1' out of the scope of claim 1, since this step of claim 1' is based on entirely the same concept of the corresponding step of claim 1, i.e., only the polysilicon on the nucleation layer(s) can be converted into single-crystal silicon.

As mentioned above, since claim 1' is within the scope of amended claim 1 but is generic to claim 11, amended claim 1 is generic to claim 11 as well as to claim 15 that has the same subject matter (OTP-ROM array process) of claim 11. Accordingly, amended claim 1 of Species 1 is generic to claims 11-19 of Species 2, and is therefore a generic claim in Group 1.

For at least the reasons mentioned above, Applicants respectfully submit that the above amendments have made claim 1 be a generic claim in Group 1, so that Species 1 and 2 no more need to be divided under 35 U.S.C. 121. Therefore, Applicants respectfully *request withdrawal of the further restriction requirement to claims 1-19 of the elected Group I.*

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CONCLUSION

Applicants have elected Species 1 of Group I. However, for at least the forgoing reasons, it is believed that Species 1 and 2 of Group I with the above amendments no more need to be divided under 35 U.S.C. 121. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted

Date : Oct. 27, 2004

Belinda Lee

Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw